IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	Before the Examiner:
Hung Q. Le et al.	:	J. Chang
Serial No.: Not Assigned	:	Group Art Unit: 2783
Filed: (herewith)	:	IBM Corporation
Title: A MECHANISM FOR SELF-INITIATED INSTRUCTION ISSUING AND METHOD THEREFOR	:	Intellectual Property Law
	:	Internal Zip 4054
	:	11400 Burnet Road
	:	Austin, Texas 78758

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

Please amend the above-identified Application as follows:

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence (along with any item referred to as being enclosed herewith) is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C 20231, on July 11, 2001.

Signature

Gracie Segovia
(Printed name of person certifying)

IN THE CLAIMS

(1) Please add new claims 38-52 as follows:

38. An apparatus for self-initiated processor instruction issuing including an issue queue, said issue queue comprising a plurality of entries, each entry of said plurality operable for containing information associated with an instruction to be issued, wherein each entry includes a first portion for storing an instruction operand and a second portion for storing a link value, and wherein, for an instruction corresponding to a first entry having a value of said instruction operand determined by an instruction corresponding to a second entry, said link value in said second entry comprises a value corresponding to a number of said first entry.

39. The apparatus of claim 38 wherein, for said first entry comprising an "*i*th" entry of said plurality of entries, said value representing said first entry is a value of an "*i*th" bit of a plurality of bits of said link value in said second entry.

40. The apparatus of claim 38 wherein each entry of said instruction queue further includes a third portion, and wherein said third portion in said first entry is operable for receiving said link value in said second entry in response to an issuing of said instruction corresponding to said second entry.

41. The apparatus of claim 40 wherein a data value in said third portion is operable for signaling an operand in a second portion of a corresponding entry of said plurality of entries is ready.

42. The apparatus of claim 38 further comprising a rename register unit coupled to said issue queue, said rename unit including a plurality of entries, said plurality of entries of said rename unit having a same number of entries as a number of entries of said instruction queue, and wherein each entry has a first portion operable for storing a data value signaling instruction information is stored in an associated entry of said plurality of entries in said issue queue.

43. The apparatus of claim 42 wherein each entry of said plurality of entries of said rename unit further includes a second portion operable for storing a pointer to said associated entry of said plurality of entries in said issue queue.

44. The apparatus of claim 38 wherein said instruction corresponding to said second entry comprises a one-cycle piped instruction.

45. A method for instruction issuing comprising the steps of:

setting a predetermined value in a first portion of an entry in an instruction queue corresponding to a first instruction in response to a dispatch of a second instruction; and

writing said predetermined value in a second portion of an entry in said instruction queue corresponding to said second instruction in response to an issuing of said first instruction, wherein a target of said first instruction comprises a source operand of said second instruction.

46. The method of claim 45 wherein said predetermined value in said first portion of said instruction queue entry is set in response to a validity value corresponding to said source operand, said validity value stored in an entry in a rename unit coupled to said instruction queue.

47. The method of claim 45 wherein said first instruction is a one-cycle piped instruction.

48. A data processing system for self-initiated instruction issuing comprising:

an instruction storage unit;

a dispatch unit coupled to said instruction storage unit;

at least one execution unit coupled to said dispatch unit for receiving instructions therefrom, each execution unit including an apparatus for issuing instructions for execution, said apparatus operable for receiving instructions from said dispatch unit, the apparatus for issuing instructions comprising an issue queue, said issue queue including a plurality of entries, each entry of said plurality operable for containing information associated with an instruction to be issued, wherein each entry includes a first portion for storing an instruction operand and a second portion for storing a link value, and wherein, for an instruction corresponding to a first entry having a value of said instruction operand determined by an instruction corresponding to a second entry, said link value in said second entry comprises a value representing said first entry.

49. The system of claim 48 wherein, for said first entry comprising an "*i*th" entry of said plurality of entries, said value representing said first entry is a predetermined value of an "*i*th" bit of a plurality of bits of said link value in said second entry.

50. The apparatus of claim 48 further comprising a rename register unit coupled to said issue queue, said rename unit including a plurality of entries, said plurality of entries of said rename unit having a same number of entries as a number of entries of said instruction queue, and wherein each entry has a first portion operable for storing a data value signaling instruction information is stored in an associated entry of said plurality of entries in said issue queue.

51. The apparatus of claim 50 wherein each entry of said instruction queue further includes a third portion, and wherein said third portion in said first entry is operable for receiving said link value in said second entry in response to an issuing of said instruction corresponding to said second entry.

52. The apparatus of claim 49 wherein said instruction corresponding to said second entry comprises a one-cycle piped instruction.

(2) Please cancel claims 7-9, 18, 20-24 and 35-37.

Respectfully submitted,

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